

REMARKS

Claims 1-20, all the claims pending in the application, stand rejected on prior art grounds. In addition, the drawings are objected to. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-20 stand rejected under 35 U.S.C. §102(e) as being anticipated by Loyer (U.S. Patent No. 6,642,742). Applicants respectfully traverse these rejections because, with the invention, the parallel combination of all the resistors is equal to the characteristic impedance of the transmission line. Since the reference voltage levels represent a virtual ground for AC analysis, the output impedance of the driver is always equal to the parallel combination of all the resistors. To the contrary, in Loyer, a specific number of transistors must be activated in order to have the output impedance of the input output circuit match the signal line.

More specifically, Loyer explains, in column 3, lines 28-33 that a specific number of resistors must be activated in order for the output impedance to match that of the signal line. To the contrary, in independent claims 1, 8, and 15 of the present invention, the "total impedance of all said resistive segments equals an impedance of said transmission line." With the invention the parallel combination of all the resistors is equal to the characteristic impedance of the transmission line. Since the reference voltage levels represent a virtual ground for AC analysis, the output impedance of the driver is always equal to the parallel combination of all the resistors (see Applicants' paragraph 23). Thus, with the claimed invention, the output level of the driver is controlled by switching selected resistors between the high and low reference level such that the parallel series combination generates the appropriate output voltage (see Applicants' paragraph 24). Regardless which resistors are connected to VH and which resistors are connected to VL the output impedance of the driver remains the same (Applicants' paragraph 28).

Quite to the contrary, Loyer requires the "activation of an appropriate number of resistive elements" in order for the output impedance to match the impedance of the transmission line (column 3, lines 28-33), while the inventive structure is designed such that the output impedance of the driver is always equal to the parallel combination of all the resistors. Therefore, with the invention, regardless which resistors are connected to VH and which resistors are connected to VL, the output impedance of the driver remains the same. Therefore, the inventive structure is superior to that structure disclosed in Loyer because with the claimed invention, the output level of the driver is controlled by switching selected resistors between the high and low reference level such that the parallel series combination generates the appropriate output voltage, and regardless which resistors are connected to VH and which resistors are connected to VL the output impedance of the driver remains the same.

Thus, while the invention allows the output level of the driver to be controlled by switching selected resistors between the high and low reference level, the output impedance of the driver remains the same because the "total impedance of all said resistive segments equals an impedance of said transmission line" as defined by independent claims 1, 8, and 15. To the contrary, with Loyer, the "activation of an appropriate number of resistive elements" is needed in order for the output impedance to match the impedance of the transmission line (column 3, lines 28-33).

Therefore, Applicants respectfully submit that Loyer does not teach or suggest that the "total impedance of all said resistive segments equals an impedance of said transmission line" independent claims 1, 8, and 15. Thus, claims 1, 8, and 15 are patentable over Loyer. Further, dependent claims 2-7, 9-14, and 16-20 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

With respect to the objection to the drawings, a Submission of Corrected Formal Drawings is submitted herewith that marks Figures 1 and 2 as prior art. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objection to the drawings.

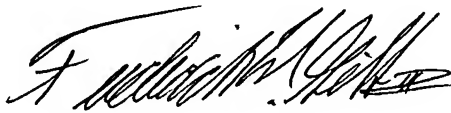
Thus, Applicants submit that claims 1-20, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 9/13/04



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Cranford, Jr. et al.

Serial No.: 10/065,475

Group Art Unit: 2819

Filed: October 22, 2002

Examiner: D. Chang

For: TERMINATING RESISTOR DRIVER FOR HIGH SPEED DATA
COMMUNICATION

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF CORRECTED FORMAL DRAWINGS

Sir:

Submitted herewith are six (6) sheets of corrected formal drawings comprising Figs. 1-10 for the above-referenced patent application. Specifically, Figs. 1 and 2 have been corrected to designate them as Prior Art. Acknowledgment of receipt is respectfully requested. Please substitute these formal drawings for the drawings which were filed on February 11, 2003.

Respectfully Submitted,

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